# Reading Between the Thermal Lines

New Dielectric Materials for LED-Packages

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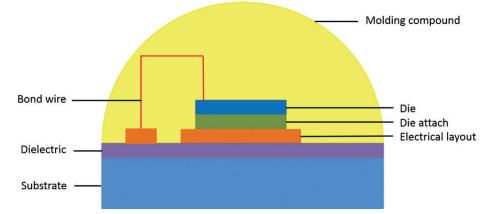




ne of the main aims in electronic packaging is a good heat transport away from the device, downwards through the package into the board. The LED chip is connected electrically at its top and bottom. That is why there is a need to separate the electric circuit from the metal board. This is achieved by an insulator layer, which is neither electrically nor thermally very conductive. In this study the thermal behavior of new dielectric materials in LED packages are investigated. Furthermore the influence of geometric parameters of the electrical layout has been tested by measurements and simulations.

Figure 1 shows the structure of a high power LED based on a chip-on-boardpackage. The chip (also called die) not only produces light, but also a certain amount of heat, which should be as low as possible. The majority of the heat from the die will be transferred to the outside by why of conduction. Since the thermal conductivity of molding compounds (e.g. epoxy or silicone) is much smaller than that of the die attach (e.g. silver conductive adhesive), most of the heat will conduct downwards. Parameters such as the thermal conductivity and the geometrical structure of the interface materials have high influences on the heat flow. So a change would lead to different measurement results with the thermal impedance test system T3ster.

Figure 2 shows the structure function of an LED package after the evaluation of the measurement. The structure function presents all the thermal information of the tested LED-package, including





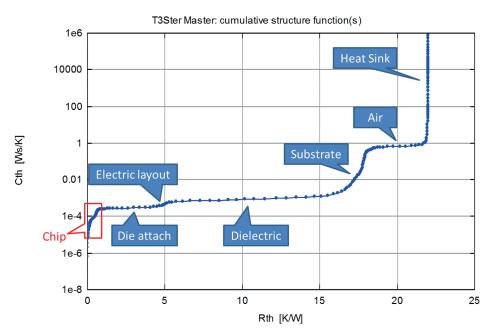


Figure 2. Structure function of an LED-Package

thermal resistance in K/W and thermal capacity in Ws/K. In fact every layer of the thermal capacity represents one kind of a material in the LED-package. The thermal resistances of different materials are of great interests to us, because the electrical components need to be cooled.

Of course a lower thermal resistance means a better performance.

#### **Electrical Layout**

Considering the electrical connection between the chip and external electrodes, the electric layout plays a very important





 $A_2$ 

Dielectric

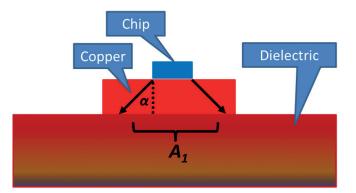


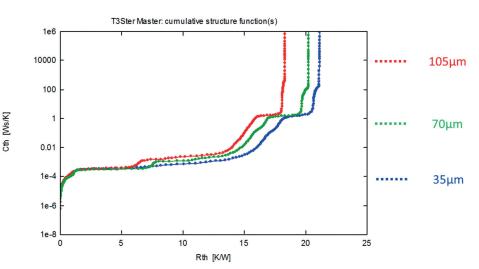
Figure 3. Heat spreading at different thicknesses of electrical layout

role in an LED package. In view of the electric conductivity and cost, copper is the first choice to the manufacturers. That is why different geometrical structures of the electric layout were built and analyzed in a thermal perspective. Beside the size of the surface, the thickness of the layout has been changed in values of 35, 70 and 105 µm. Copper has a high thermal conductivity of  $\lambda$ =385 W/mK. For a copper layout with a surface area of 5 mm x 5 mm and a thickness of 35 µm, the thermal resistance is  $R_{\rm th} = \frac{1}{\lambda \cdot A} = 0.0036$  K/W.

This value is so small that a triplication of the thickness to 105 µm leads to only 0.01 K/W. So, why the concern over thickness? The answer lies in the effect of heat spreading, which is not represented by the formula above, but rather detected in measurement results. Figure 3 shows the approach of the effect by using a refraction model [1].

The die's heat flow reaches the copper layer and will be spread in this material. Compared to optics the refraction at the boundary surface is dependent on the refraction index, which is the conductivity in the thermal picture. The chip's junction to a high conductive material means a high refraction angle a, so that a high spreading effect should appear. By increasing the copper layout's thickness, the surface A, which is flown through by the heat, gets larger. Now, we can calculate the next thermal resistance with the simple formula again. The experimental results and transient thermal simulation with FIoTHERM are shown in the following figures 4 and 5.

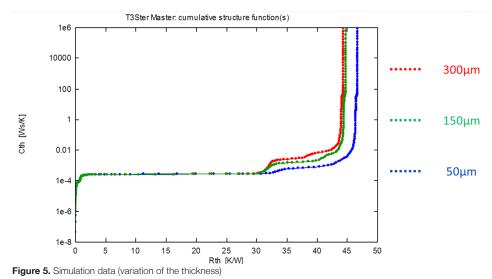
Both results confirm that the total thermal resistance with a thicker copper layout is lower. That is because heat flows into the dielectric with a higher surface area (Figure 3). So the dielectric itself has a



Chip

Copper





smaller thermal resistance. Since a thicker thickness means more material, a higher thermal capacity should be observed. Since very thin layers mean a long simulation time, the thicknesses of glue and dielectric differ to the test devices. The trend of lower thermal resistance and higher capacity by enlarging the copper layout's thickness appears in measurement and simulation data.

#### **New Dielectric Materials**

All used dielectric are based on polymer and/or ceramic materials. The techniques to connect the dielectric layer with the board's substrate and electrical layout differ. A standard method, is laminating



the electrical layout on a ceramic filled polymer by an epoxy adhesive. Since the thermal conductivity of polymer is lower than that of ceramic, a new approach is to use a ceramic layer that consists of nano-crystalline aluminum oxide crystals (Al2O3) [2]. The electrical layout is laminated on this pure ceramic layer, or even contacted directly by a metallization process.

Samples with the same LED package, but different dielectrics are tested with the thermal impedance measurement. A direct comparison of Nanotherm LC and a ceramic paste (Figure 6) as well as Nanotherm DM and a ceramic filled polymer has been made. Figures 8 and 9 show the results of the measurement's structure functions.

Thermal resistances of dielectric and substrate build the main part of the total thermal resistance in the investigated LED-package. The use of a laminated nano-ceramic instead of a ceramic paste reduces the thermal resistance from 40 to 10 K/W (Figure 8). One reason for this is the small thickness of the ceramic layer (10 µm). The direct comparison of pure nano-ceramic with a laminated ceramic filled polymer of a standard PCB also shows a reduction of the dielectric's thermal resistance of about 33%. The conductivity is higher and the thickness of the direct metallized material is smaller, so the consequence must be a reduction in the total thermal resistance.

#### Conclusion

Not every transient behavior can be covered by a simple one-dimensional calculation. Heat spreading effects in

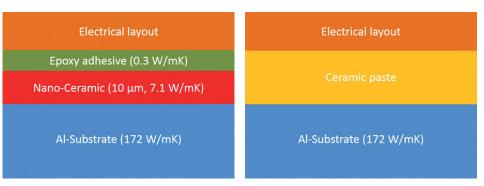


Figure 6. Comparison of Nanotherm LC (Laminated Circuit) and ceramic paste [3]

Electrical layout	Electrical layout
Nano-Ceramic (10 µm, 7.1 W/mK)	Epoxy adhesive (0.3 W/mK)
Al-Substrate (172 W/mK)	Ceramic filled polymer (75 µm, 2.2 W/mK)
	Al-Substrate (172 W/mK)

Figure 7. Comparison of Nanotherm DM (Direct metallization) and ceramic filled polymer [3]

the electrical layout directly affect the measurement curves and must be considered by other models. The change of the PCB's dielectric has the biggest effect on the total thermal resistance. Beside a standard ceramic filled polymer, new dielectric materials are tested. A direct comparison of laminated and direct metallized Nanotherm, and the aging behavior and reliability of both materials are interesting aspects that should be studied in the future.

#### **References:**

[1] David P. Kennedy. "Heat conduction in a homogeneous solid circular cylinder of isotropic media". Product Development Laboratory, Data Systems Div., International Business Machines Corp, Poughkeepsie, NY, 1959.

[2] http://www.camnano.com

[3] Data sheet from Excelitas Technologies and Cambridge Nanotherm.

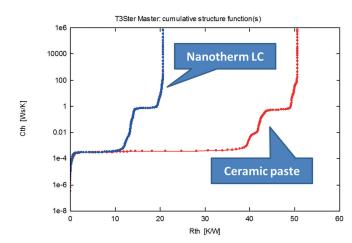


Figure 8. Structure functions of Nanotherm LC and a ceramic paste as dielectric material

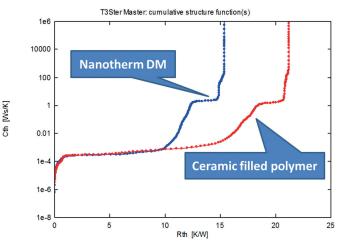


Figure 9. Structure functions of Nanotherm DM





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