HOW TO PREDICT COMPONENT TEMPERATURES FOR COMPLEX NETWORK AND TELECOMMUNICATIONS EQUIPMENT

WHITEPAPER

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MECHANICAL ANALYSIS

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The insides of network and telecom equipment consist of a complex assembly of many solid objects (PCBs, electronics packages and devices, cabling, fans, and heatsinks, for example). Airflow is confined within narrow regions between these solid objects, and airflow (convective transport) affects temperature which affects reliable operation. In addition, conduction within the solid objects, which also can have extremely complex internal structures, affects how these components will operate.

Thermal analyses involve large numbers of such objects (sometimes thousands), as well as extreme disparities in scale (from meter scale rack systems to micron scale PCB traces). Because of this complexity, these electronic products pose a unique set of challenges for thermal simulation, such as geometry capture, scale disparity, uncertainty over missing data (for example, component thermal data, power dissipation, material properties, layer thicknesses, interface resistances), transitional flow regime, mesh generation, hardware environment, and the increasing need for greater accuracy.

Mentor Graphics addresses this challenge by providing thermal simulation and analysis software using computational fluid dynamics (CFD), and thermal characterization hardware tools. This paper talks about how to optimize the thermal design of electronic network and communications equipment by modeling and analyzing internal component temperatures using some of these tools.

REMOVE UNCERTAINTY WHEN PREDICTING COMPONENT TEMPERATURES

Component temperature usually has been correlated with reliability. More recently physics-based reliability prediction has related failure rates of electronic assemblies to the magnitude of temperature change over an operational cycle (power-on, power-off, power-on…), and rate of temperature change, both of which are influenced by steady-state operating temperature. Failures are often attributed to solder joint fatigue.

In some applications, such as computing, CPU speed is adversely affected by temperature, and in some situations, components have to run at very similar temperatures to avoid timing issues. High temperatures can cause operational issues, such as latch-up. Whether the intention is to increase reliability, improve performance, or avoid problems during operation, accurate prediction of component temperatures helps thermal designers to achieve their goals.

Reliable, accurate prediction of component temperatures enables understanding of how close the design values come to the maximum allowable temperature.

START WITH 3D COMPONENT MODELS AND THEN REFINE THE COMPONENT THERMAL MODEL

It's important to include some form of 3D component model in the simulation before finalizing on a component during equipment design. In this way, thermal performance can be considered as part of a package selection criteria. Some ICs are available in more than one package style, and not all package styles perform equally well from a thermal point of view. The need for adding a heatsink later on in the design may be eliminated by appropriate package selection.

Component temperature, either in the form of a case temperature or junction temperature depending on how the manufacturer has specified the component, is the key measure used to indicate whether the design is acceptable from a thermal perspective. At this stage, however, only a rough estimate of component temperature is obtainable.

In the absence of any other information, the simplest 3D component model that can be used is a conducting block. The FloTHERM® 3D thermal simulation software includes material properties that are tailored to give a case temperature prediction for different package styles.

For plastic components, a thermal conductivity of 5 to 10 W/mK is recommended [1], and 15 W/mK for any ceramic components. The lowest conductivity is a worse-case for case temperature.

By representing the package body in 3D, the effect of the component on the local airflow, and correspondingly any downstream components, is taken into account. Large components can shield smaller, lower profile components from cooling air, and the wake formed behind a component is a region in which the same air gets recirculated, so any components in that region are likely to be hot.

Try to align any rectangular components so that their long side is parallel to the primary flow direction. This both reduces the overall pressure drop because the flow "sees" less of an obstruction and produces a smaller wake, minimizing the effect on downstream components.

In early design, for example before a PCB is routed or the number of layers in the board is known, accurate component temperature prediction is not possible, and a thermally sophisticated model of the component is not called for. But later in the design when the model of the board can be refined, it's important to also refine the component thermal model.

Choices about the most appropriate component thermal model are iterative because components that are predicted to be hot [1] indicate the need to both refine the component's thermal model and to perhaps consider a component-specific thermal management solution.

USE RELEVANT THERMAL METRICS TO COMPARE THERMAL PERFORMANCE OF COMPONENTS

For components without a heatsink, the most relevant thermal metric to compare is the junction-to-board resistance [2]. For components that are expected to have a heatsink, the junction-to-case resistance is the most relevant because the resistance is usually defined for the face that is in contact with the heatsink [3]. For TO type packages, this face is normally soldered to the PCB. If both of these metrics are available, a JEDEC standard 2-resistor model can be created and the thermal model re-run to get a first estimate of junction temperature [4].

2-RESISTOR COMPACT THERMAL MODELS

A 2-resistor compact thermal model (CTM) is the lowest fidelity model that is capable of predicting both case and junction temperatures. It does not require any more mesh than a simple conducting block, so using 2-resistor models does not affect simulation time. Although this has the lowest computational burden, the worse-case error in junction temperature prediction can be as high as ±30% and varies with both package type and package size.

The junction-to-case resistance and junction-to-board resistance thermal metrics this model is based on are measured under standardized conditions. The JEDEC Standard JESD15-3 requires the junction-to-board resistance to be measured on a 2s2p board with continuous power and ground planes. The junction-to-case resistance is measured by pressing the top of the package against a cold plate. As a result, the predictive accuracy of the 2-resistor model is higher the more closely the application resembles the test conditions.

For the junction-to-case resistance, the application environment that most closely corresponds to the test environment is when the component has a heatsink that covers the whole of the package surface. For this reason, 2-resistor models can be used to initially assess the size of heatsink required. The top surface of a 2-resistor model is an isothermal node representing the case so that the base of the heatsink will be isothermal. Therefore, a 2-resistor model can be used to determine the number of fins, fin thickness, and fin height needed to reduce the air-side thermal resistance of the heatsink, but it cannot be used to determine the base thickness needed to adequately spread the heat that will ensure that heat passing to the outer fins is not overly restricted.

RC-LADDER MODELS

For packages that have a single heat flow path, such as LEDs and TO-style packages, there is a JEDEC standard approach [1] for measuring a thermal resistor-capacitor model of the heat flow path from the junction down to the package tab. This method does not directly provide a thermal resistance to the exposed top surface of the package. However, T3Ster, Mentor Graphics transient thermal tester, can be used to create an RC-ladder thermal

model that takes this into account. T3Ster is the industry-leading solution for measuring packaged ICs to create these thermal models, which can then be used directly as a network assembly for 3D thermal simulation in FloTHERM. Unlike 2-resistor models that only contain thermal resistors, RC-ladder models include thermal capacitors, and thus they can be used for transient simulations. These models can provide excellent results when the application environment is close to that of the test cold plate environment, for example, when the package is soldered to a MCPCB or a copper pad on a high conductivity board.

DELPHI MODELS

The next level up in terms of predictive accuracy is a DELPHI model [5]. These models have partitioned top and bottom surfaces, with a matrix of thermal resistors to connect these surfaces to the junction and/or to one another. The additional internal thermal resistors allow the heat flow through these paths within the package to adjust depending on the boundary conditions. In many applications, the model will predict the junction temperature to ±10% accuracy, being a worse-case figure. DELPHI models are adequate for detailed thermal design work of all but the most thermally critical packages, stacked or 3D ICs, or where additional information is needed from the simulation, such as temperature distribution on the die surface.

DELPHI models are better for heatsink selection than 2-resistor models because they can be used to initially investigate the effect of the thickness of the heatsink base. However, for thermally critical packages that require a heatsink, the use of a detailed model is recommended.

READILY AVAILABLE MODELS

It is also well worth doing an Internet search for the components datasheet and to see if there are any FloTHERM models available and if not request a FloTHERM model from your supplier. Sometimes these are provided under a non-disclosure agreement. Many of the leading IC package vendors provide thermal models for FloTHERM. And systems integrators use FloTHERM PACK's JEDEC Package wizard to generate a representative thermal model of the package simply by knowing the package style, body size, and number of leads. FloTHERM PACK also provides access to all the input data, so the model can be updated when more information about the package becomes available, and it generates 2-resistor, DELPHI, and detailed models for easy refining of the component thermal model as the design is elaborated.

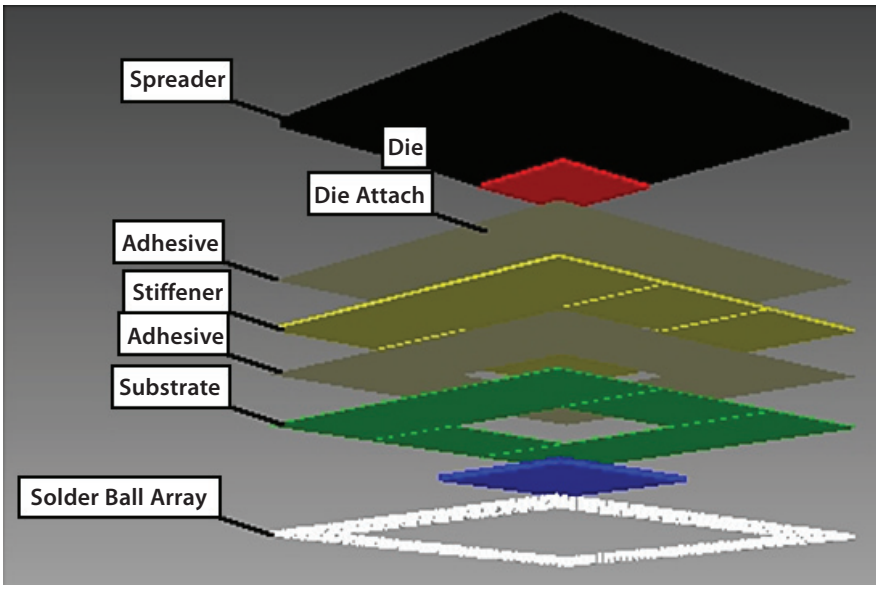

Figure 1: Detailed Thermal Model of a Chip Package

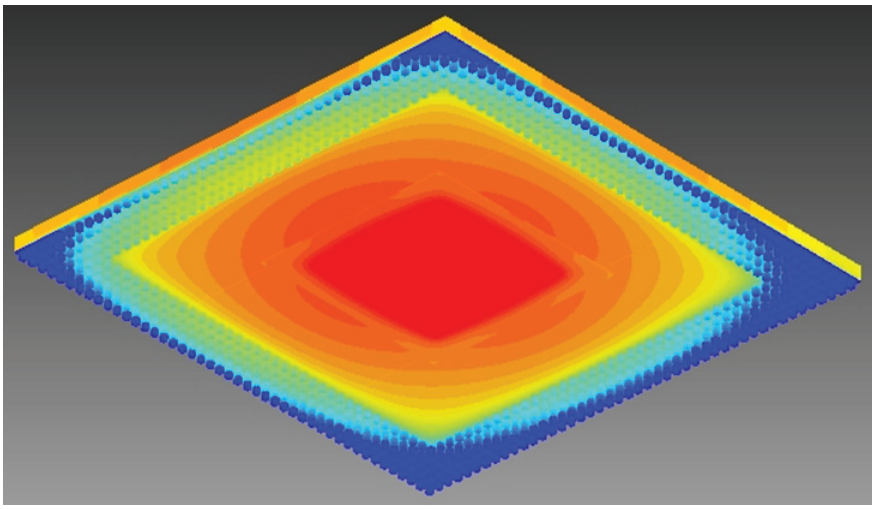

Figure 2: Temperature Distribution on Underside of a BGA Package showing Solder Balls

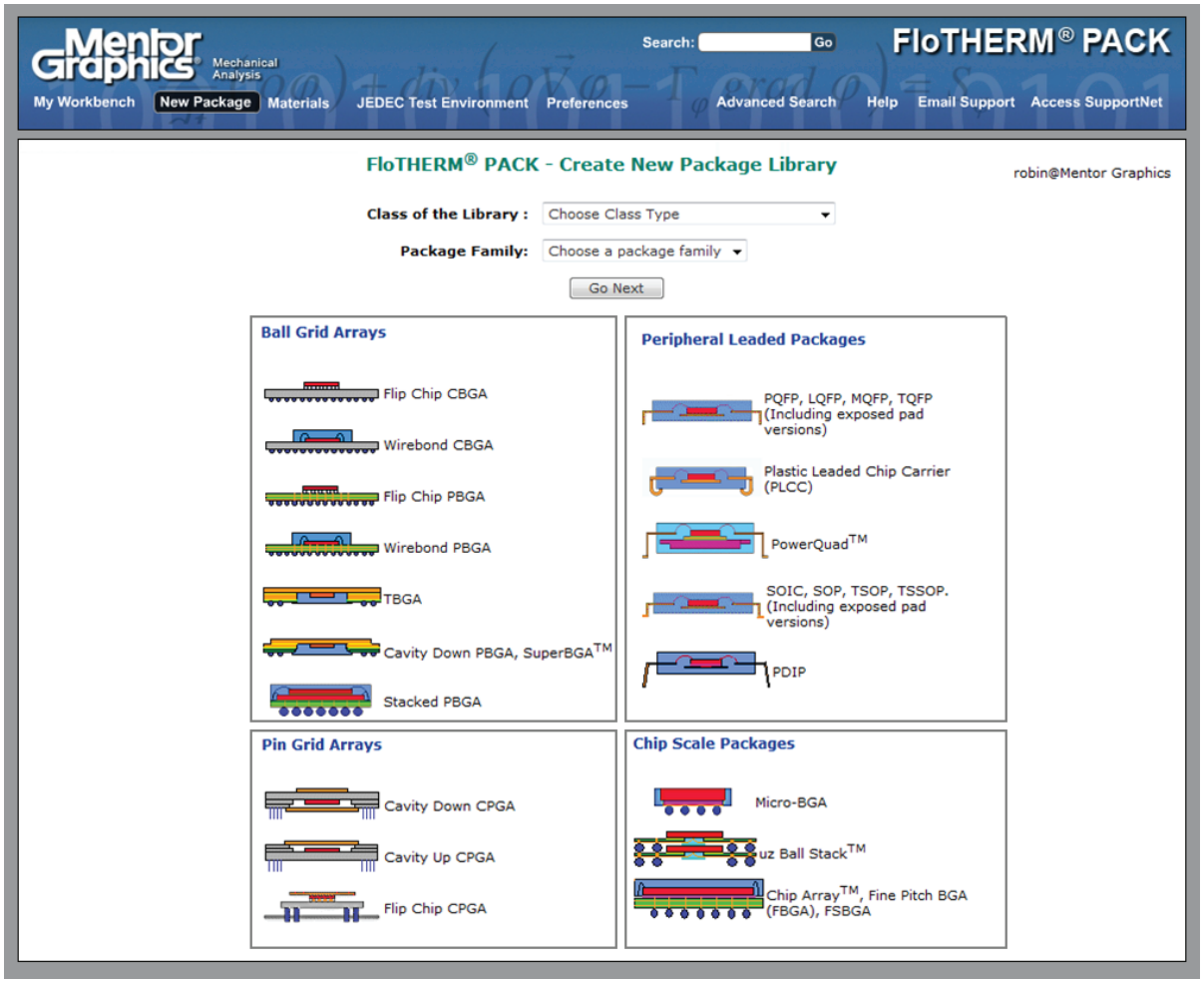

Figure 3: FloTHERM PACK

USE POWER MAPS TO PREDICT TEMPERATURE VARIATION

As dies get thinner, temperature variation across the die surface increases because the die becomes less effective as a heat spreader. Consequently, it is becoming more common to consider junction temperature as a variable number over the surface of the die, rather than a single number. However, when using compact models, junction temperature is considered a single value, and the model, if provided by a vendor, should provide the number that is appropriate to compare against the specified maximum allowable junction temperature. The maximum junction temperature usually has to be limited.

Detailed models predict the temperature variation throughout the package, including the die. The active power variation over the die's active surface has to be accounted for to accurately predict the temperature distribution on the die. For more complex die (such as system-on-chip, SoCs) this is often a function of what the die is doing, so a die may well have several power maps associated with it. In addition, leakage power is a function of the local temperature, and thus it is exacerbated by the active power.

Power maps can be exported from power analysis tools and may be available as a comma-separated variable (CSV) file. These are often coarsened by the vendor to provide a power map with typically up to ~50 different power regions.

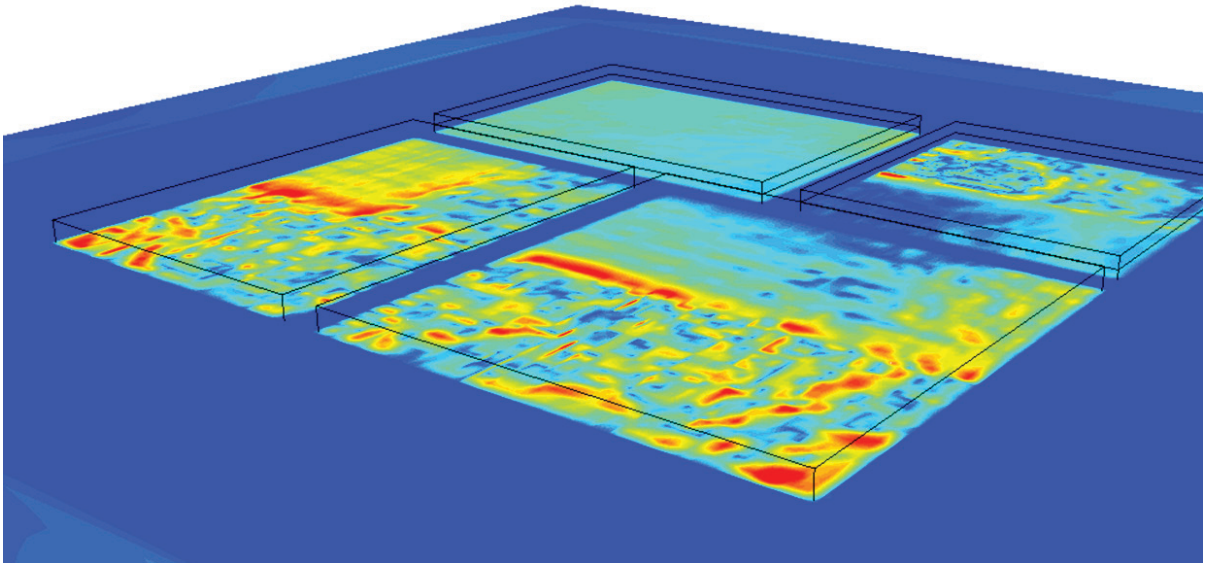

Figure 4: Detailed Model of a Multi-Chip Package with Die Power Maps

Monitor points should be used to monitor the temperature of the center of the regions found to have the highest temperature from a steady-state simulation with each power map.

VALIDATE DETAILED MODELS WITH EXPERIMENTS

Transient thermal testing techniques allow the effective thermal resistances and capacitances in the model to be calibrated against experiment. Uncertainties can be addressed by using T3Ster to measure the response of an actual package, and then the simulation model can be adjusted to fit the experimental response. In this way, the junction temperature rise within the package can be predicted to within just a few percent for all boundary conditions and at all times during a transient simulation, which is the pinnacle of package thermal modeling.

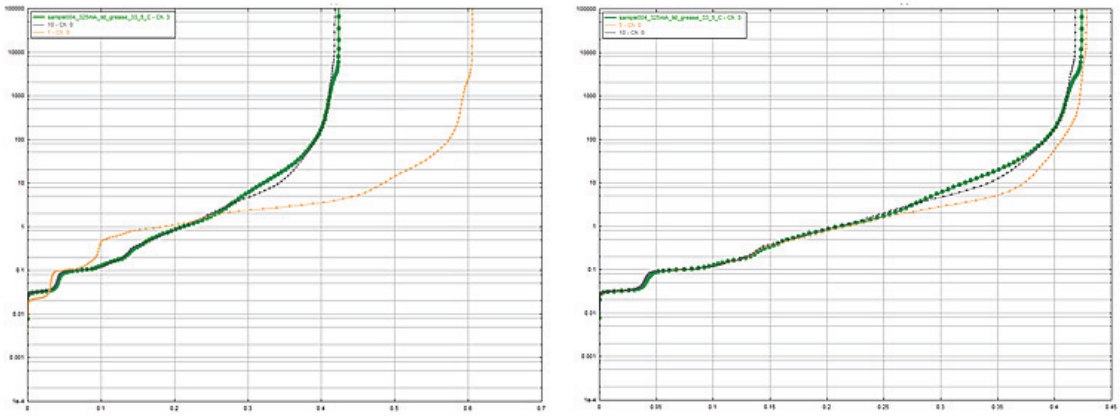

Figure 5: Initial vs Final Structure Function Fits for a Package [Ref. 4].

For package designers, a validated detailed thermal model is a prerequisite for subsequent improvements in design, materials, and processing. Finite-element based stress prediction depends on ensuring the correct temperature distribution within the package and its warping and structural interaction with the PCB. Also a validated detailed thermal model is the best starting point for any custom heatsink design.

DESIGN BETTER HEATSINK SOLUTIONS FOR COOLING COMPONENTS

Often early in the design process, a standard heatsink is selected to ensure that the component can be adequately cooled, but it may be a suboptimal solution. Instead, optimizing a custom heatsink design maximizes the heat transfer for the minimum system pressure drop and wake region formed behind the heatsink. For large packages, the contact area between the heatsink and the package body also can be optimized to prevent heat spreading in the base of the heatsink and then flowing back into the package body around its periphery.

KNOW THE TIM RESISTANCE TO ACCURATELY PREDICT COMPONENT TEMPERATURE

The thermal conductivity of the thermal interface material (TIM) can be accurately measured as a function of temperature by using the specialized T3Ster DynTIM tool to help choose the most suitable TIM material for a particular application, such as between a component and a heatsink. The total thermal resistance depends on how well the chosen material wets the surface as this affects the interfacial resistances on each side of the TIM. The thermal resistance of the TIM can be a substantial contribution to the junction temperature rise; thus, accurate data for the overall TIM thermal resistance is important for accurate component temperature prediction.

PROVIDE ACCURATE TEMPERATURES FOR MECHANICAL STRESS PREDICTION

As IC packaging challenges continue to increase, package vendors are finding the need to design for thermally induced stresses that more closely match those the part will experience in the application environment.

From Version 10 of FloTHERM, assembly temperatures can be exported for use in a finite-element stress tool to provide the thermal strain as a boundary condition for the stress calculation. Temperatures are intelligently mapped

onto the finite element mesh accounting for differences in the shapes of the geometric objects that might exist between the two analysis disciplines. The assembly under consideration can for example include the package, heatsink if attached, and a section of the board onto which the part is soldered.

EXAMPLE: USING FLOTHERM TO OPTIMIZE COMPONENT PLACEMENT FOR A HIGH-SPEED SWITCH

The design team working on the Alcatel 1678 Metro Core Connect (MCC) high-speed optical networking switch, which provides 640 Gb/s capacity in one shelf, recognized that they needed to address the cooling issues starting from the very beginning of the project.

The switch features high switching capacity and high-density interfaces within a very compact package. Thermal management presented a major design challenge because the switch used as much as 2000 W per shelf and 140 W for each plug-in card. The use of high-speed optical transceivers and ASICs with restricted temperature ranges increased the difficulty of the design challenge.

The team performed a shelf-level simulation with FloTHERM, using airflow measurements to define environmental conditions. They built detailed and compact thermal simulation models of all relevant ASICs and of the optical transceivers with FloTHERM and FloTHERM PACK. Some of their models were provided by component suppliers.

Their analysis results were used optimize the component placement, maximize the air flow to critical components and design highly efficient heatsinks for cooling hot spots. The team solved all thermal issues at an early stage of the design process and the required changes could be made easily and inexpensively.

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